Reg. No. : | | | | | | | | | | | |

Question Paper Code : P 1263

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2009.

Fourth Semester

Electronics and Instrumentation Engineering

EC 1312 — DIGITAL LOGIC CIRCUITS

(Common to Instrumentation and Control Engineering)

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Show that $A(A + B) = A$.

2. Convert the binary $[10101101]_2$ into its Gray code.

3. Give an application each for a multiplexer and a demultiplexer.

4. Give an application for XOR function.

5. State the problem normally encountered in SR flip flop.

6. How many flip-flops are needed to realise a mod-16 counter?

7. What is an asynchronous sequential circuit?

8. What is a PLA?

9. Define fan-out.

10. Define noise-margin.

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the following using K-map and realise the reduced function using NAND gates

$\sum m(0, 1, 3, 5, 6, 8, 9, 14, 26, 28, 31) + \sum d(4, 13)$.

Or

(b) Simplify the following using Quine Mccluskey method and realise the reduced function using NAND gates

$\sum m(1, 2, 4, 5, 7, 9, 12, 13) + \sum d(3, 8)$.

12. (a) Design the following circuits

(i) Full adder (8)

(ii) 1-4 demultiplexer. (8)

Or

(b) (i) Implement the following function using a multiplexer

$F(A, B, C) = \sum(1, 3, 5, 6)$. (6)

(ii) Design a 3-to-8 decoder. (10)

13. (a) (i) Explain the working of a master-slave JK flip-flop. (8)

(ii) Design a mod-7 counter. (8)

Or

(b) Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 1011 is detected.

14. (a) Design an asynchronous sequential circuit that has two inputs x_1 and x_2 and one output z. The output $z = 1$ if x_1 changes from 0 to 1, $z = 0$ if x_2 changes from 0 to 1 and $z = 0$ otherwise. Realise the circuit using D-flip-flops.

Or

(b) Design an asynchronous circuit that will output only the second pulse received whenever a control input is asserted from LOW to HIGH state and will ignore any other pulse.

15. (a) (i) Explain the working of a two input TTL NAND gate. (10)

(ii) Write notes on FPGA. (6)

Or

(b) (i) Explain the working of a two input CMOS NAND gate. (10)

(ii) Compare the performance of various digital logic families. (6)