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Question Paper Code : Q 2211

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2009.

Eighth Semester

Electrical and Electronics Engineering

EC 1461 — VLSI DESIGN

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Mention with necessary expressions why NMOS is used as a pull down and PMOS used as a pull up device.

2. Give the expressions for noise margin high NM_H and noise margin low NM_L for a CMOS inverter circuit.

3. Implement the following Boolean expression using full static CMOS logic.

   Y = (A.B) + (D.B.C) + (D.A) + (A.C.B).

4. Give the expression for computing dynamic power dissipation in CMOS logic circuits.

5. Realize OR and NOR logic function using differential cascade voltage switch logic.

6. Define the setup time for a register.

7. Differentiate FPGA from PLA.

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8. Determine the logic function F for the logic circuit given in figure 1.

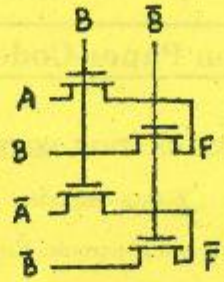

Fig. 1

9. What is meant by standard cell design?

10. Differentiate sequential and concurrent statements in VHDL.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw the V I characteristic for an NMOS transistor showing various region of operation. (6)

(ii) Derive the first order ideal drain current equation describing the subthreshold region, triode region and saturation region for an NMOS transistor. (10)

Or

(b) Describe the following second order effects experienced in MOS transistor, with necessary expressions.

(i) Body effect

(ii) Channel length modulation

(iii) Fowler nordheim tunneling

(iv) Hot electrons.

12. (a) (i) Derive and draw the voltage transfer characteristic curve for a CMOS inverter showing the five regions of operation. (10)

(ii) Draw the stick diagram for a 3-input NOR gate. (6)

Or

(b) (i) Derive and compare VOH, VOL parameters for a pseudo-nMOS inverter and saturated load inverters. (8)

(ii) Determine VOH, VOL for a BICMOS inverter and draw its voltage transfer characteristic. (8)

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13. (a) (i) Mention the features of dynamic CMOS logic circuits. (6)

(ii) Explain why dynamic logic circuits cannot be cascaded directly. Give alternative circuits to cascade dynamic logic circuits. (10)

Or

(b) (i) Implement XOR logic function using pass transistor logic and mention the limitations in the circuit . Give alternative circuit techniques to overcome those limitations. (8)

(ii) Give the circuit diagram for a 4-bit barrel shifter. Explain one shift left operation with specific example. (8)

14. (a) Implement the following Boolean expression using pseudo nMOS PLA architecture

$Z_0 = -x_1 . x_3$; $Z_1 = -x_1 + (-x_0 . x_2 . x_3)$; $Z_2 = -x_3$;

$Z_3 = (-x_1 . x_2 . -x_3) + (-x_0 . -x_2 . x_3)$.

Or

(b) Explain for any FPGA device, in general its architecture, the configurable logic blocks, interconnecting schemes, I/O modules.

15. (a) Using structural level VHDL coding, realize a 4-bit adder. Write a test bench to define the stimulus for the 2-inputs for the 4-bit adder.

Or

(b) Using sequential statements describe a pulse generator in VHDL. Write a test bench to define the stimulus for the pulse generator.

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