Reg. No. : | | | | | | | | | | | |

Question Paper Code : P 1274

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2009.

Seventh Semester

Electronics and Communication Engineering

EC 1401 — VLSI DESIGN

(Common to B.E. (Part-Time) Sixth Semester Regulation 2005)

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the different MOS layer ?
2. What are the two types of layout design rules?
3. Define rise time and fall time.
4. What is a Pull down device?
5. What are the differences between tasks and function?
6. What is the difference between = = = and = =?
7. What is CRC?
8. Draw an nassert high switch condition if input = 0 and input = 1.
9. What do you mean by DFT?
10. Draw the Boundary scan input logic diagram.

PART B — (5 × 16 = 80 marks)

11. (a) Discuss the steps involved in IC fabrication process. (16)

Or

(b) Describe n-well process in detail. (16)

12. (a) (i) Explain the DC characteristics of CMOS inverter with neat sketch. (8)

(ii) Explain channel length modulation and body effect. (8)

Or

(b) (i) Explain the different regions of operation in a MOS transistor. (10)

(ii) Write a note on MOS models. (6)

13. (a) Explain in detail any five operators used in HDL. (16)

Or

(b) (i) Write the verilog code for 4 bit ripple carry full adder. (10)

(ii) Give the structural description for priority encoder using verilog. (6)

14. (a) Explain in detail the sequence of steps to design an ASIC. (16)

Or

(b) Describe in detail the chip with programmable logic structures. (16)

15. (a) Explain in detail Scan Based Test Techniques. (16)

Or

(b) Discuss the three main design strategies for testability. (16)