Reg. No. : | | | | | | | | | | | |

Question Paper Code : P 1264

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2009.

Fifth Semester

Electrical and Electronics Engineering

EC 1312 — DIGITAL LOGIC CIRCUITS

(Common to B.E. (Part-Time) Fourth Semester Regulation 2005)

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Perform (11011–100101) using 2's complement method.

2. Distinguish between completely specified function and incompletely specified function.

3. What is a priority encoder?

4. Draw a 4 × 16 decoder constructed with two 3 × 8 decoders.

5. Give the state diagram of JK FF.

6. Differentiate a latch and a flip flop.

7. What is meant by asynchronous sequential machine?

8. Determine the maximum number of binary states and the largest number that can be counted by 5FF and 6FF configuration.

9. What is the effect of increasing the supply voltage on the propagation delay of the CMOS gates?

10. How does open collector outputs differ from the totem-pole outputs?

PART B — (5 × 16 = 80 marks)

11. (a) Obtain the minimum SOP using Quine McClusky's method and verify using K-map.

$$F = m_0 + m_2 + m_4 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13}.$$

Or

(b) (i) Reduce the following using K-map.

$$F = m_2 + m_3 + m_4 + m_6 + m_7 + m_9 + m_{11} + m_{13}. \quad (6)$$

(ii) State and prove De Morgan's theorem. (10)

12. (a) (i) Construct a BCD to Excess-3 code encoder. (8)

(ii) Implement a full adder using half adders. (8)

Or

(b) Minimize and implement the following multiple output functions in SOP form (8 + 8)

$$f_1 = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 4, 5, 14, 15).$$

$$f_2 = \sum m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12).$$

13. (a) Design a synchronous counter using JK FF to count the following sequence.

7, 4, 3, 1, 5, 0, 7...

Or

(b) Design a sequential circuit with 4FF ABCD. The next states of B, C, D are equal to the present states of A, B, C. The next state of A is equal to the EX-OR of the present states of C and D.

14. (a) Design an asynchronous sequential machine that will permit passage of a complete single clock pulse from a continuous stream of input clock pulses, when an external input signal is high, the machine is to ignore the case when both the input clock and the control signal go high at the same time.

Or

(b) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. The output is to remain a '0', as long as X_1 is '0'. The first change in X_2 that occurs while X_1 is a '1' will cause Z to be a 1. Z is to remain a 1 until X_1 returns to zero.

15. (a) Describe the following digital circuits :

(i) FPGA. (8)

(ii) EPROM. (8)

Or

(b) Write detailed notes on the working and characteristics of the following logic families.

(i) ECL (8)

(ii) CMOS. (8)