Reg. No. : | | | | | | | | | | | |

**Question Paper Code : P 1201**

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2009.

Third Semester

(Regulation 2004)

Computer Science and Engineering

CS 1202 — DIGITAL PRINCIPLES AND SYSTEMS DESIGN

(Common to B.Tech. Information Technology)

(Common to B.E. (Part-Time) Second Semester (Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State and prove De-Morgan's law.
2. Name the various types of number systems with their bases and give an example for each.
3. What are the advantages of tri-state gates?
4. What is HDL?
5. Distinguish between a decoder and a demultiplexer.
6. How is division operation performed using a subtractor?
7. Give any two applications of a Shift Register.
8. What is Triggering? What is the need for a trigger in a flip-flop?
9. What are Race free assignments?
10. What is a hazard free network?

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PART B — (5 × 16 = 80 marks)

11. (a) (i) Use Boolean theorems and simplify the following :

(1) $A'BC'+ABC+A'B'C'+A'B'C+AB'C'+A'BC'$. (4)

(2) $(A+B'+C)(A'+B'+C)(A+B+C)(A'+B+C')$. (4)

(ii) State and prove the various Boolean Theorems. (8)

Or

(b) Simplify the following expression.

$y=m1+m3+m4+m5+m8+m9+m10+m11+m12+m14$ using

(i) Karnaugh map. (8)

(ii) Quine Mcluskey method. (8)

12. (a) What are Universal gates? Represent all the gate operations with universal gates. (16)

Or

(b) What is a Combinational circuit? Explain with various circuits of how arithmetic operations are performed. (16)

13. (a) Design a full adder and a full subtractor and implement it with a suitable decoder. (16)

Or

(b) (i) Explain how HDL is used for combinational circuits. (8)

(ii) Explain the functionality of a multiplexer to get 12 outputs. (8)

14. (a) Design and explain an asynchronous master slave JK-flip-flop and give its truth table. (16)

Or

(b) Explain how shift registers are useful in performing arithmetic operations. (16)

15. (a) Explain how state reduction in flow tables is performed using asynchronous sequential circuits. (16)

Or

(b) Design and explain Fundamental mode and pulse mode sequential circuits. (16)

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