Reg. No. : | | | | | | | | | | | |

Question Paper Code : Z 7458

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2009.

Elective

VLSI Design

VL 1622 — LOW POWER VLSI DESIGN

(Common to M.E. Applied Electronics)

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Why power dissipation is recognized as a critical parameter in modern VLSI design field?

2. What is the difference between power and energy?

3. What is logical level optimization?

4. Give the advantages of static Vs dynamic logic.

5. Which logic style is more reliable – Static or Dynamic?

6. What are the common principles for low power design that are applied to arithmetic circuits?

7. Define signal probability.

8. What is Reconvergent Fanout Region?

9. What are the software sources of power dissipation?

10. What is instruction level power analysis?

PART B — (5 × 16 = 80 marks)

11. (a) Explain the components of power dissipation in CMOS circuits. (16)

Or

(b) (i) What are the principles of low power design? (8)

(ii) Write about the significance of reduction of both active power and standby power. (8)

12. (a) Explain the optimization techniques for combinational circuits. (16)

Or

(b) Explain the optimization techniques for sequential circuits. (16)

13. (a) Explain the several logic styles in terms of performance, area and power consumption. (16)

Or

(b) Explain the power characteristics of latches, flip-flop and memories. (16)

14. (a) (i) What is signal correlation? Write about the impact of signal correlations at the switching activity. (8)

(ii) Give the classification of power estimation methodologies. (8)

Or

(b) (i) Explain Monte Carlo based power estimation method. (8)

(ii) What is zero delay power estimation? (8)

15. (a) Explain the synthesis and optimization procedures for low power dissipation at the algorithm, architecture and logic levels. (16)

Or

(b) Explain the software optimizations for minimum power. (16)

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